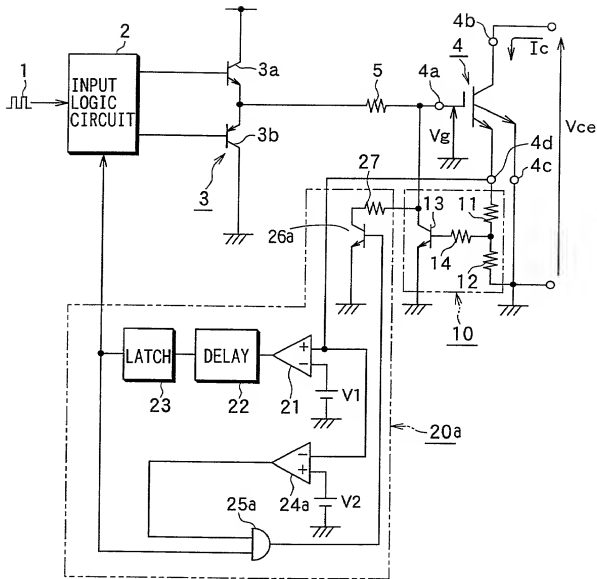


FIG. 1



00019715-000001

FIG. 2A

I_c

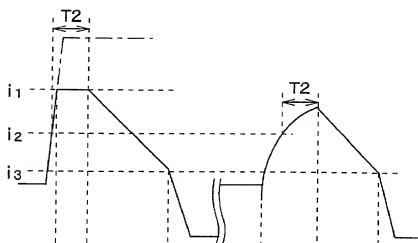


FIG. 2B

OUTPUT OF
LATCH CIRCUIT

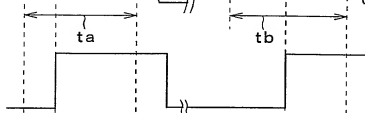


FIG. 2C

V_g

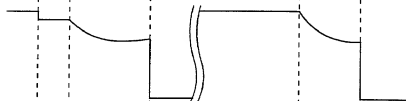


FIG. 2D

V_{ce}

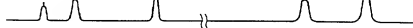


FIG. 3

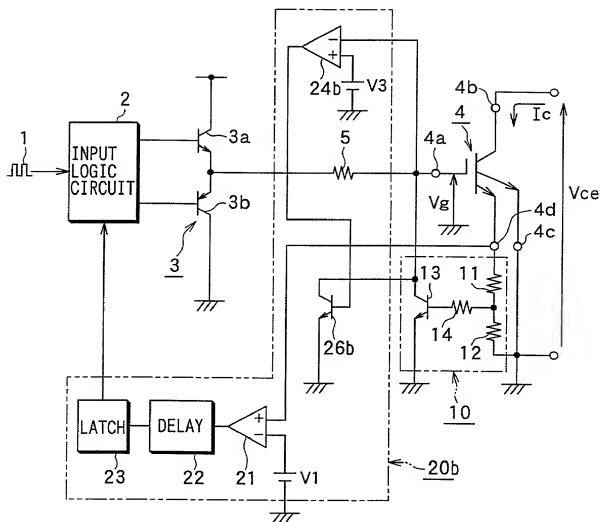


FIG. 5A

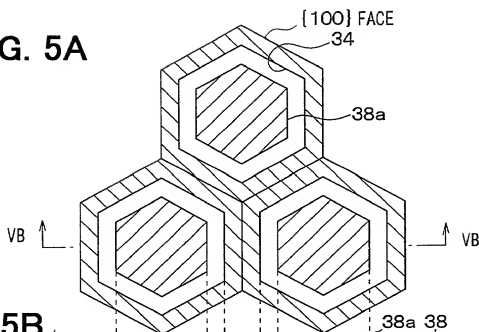


FIG. 5B

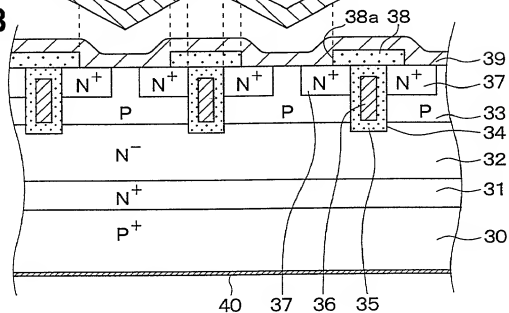


FIG. 6

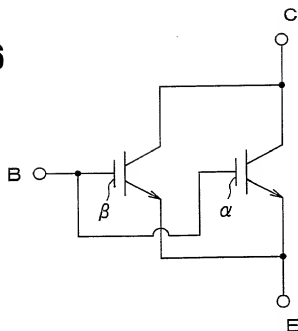


FIG. 7

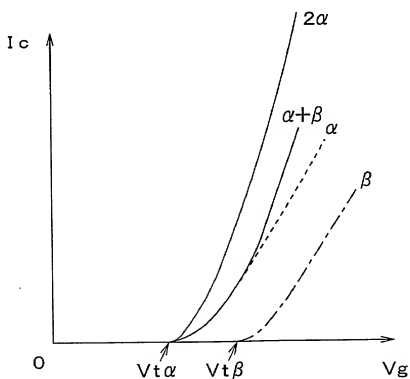


FIG. 8

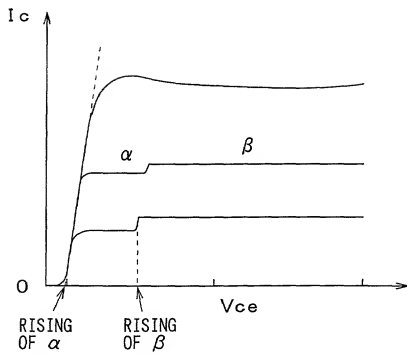


FIG. 9A

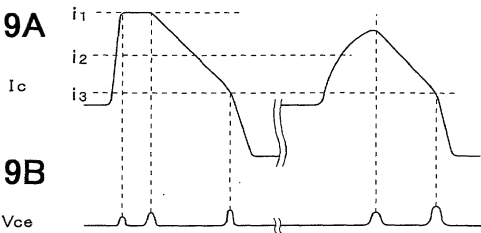


FIG. 9B

FIG. 10A

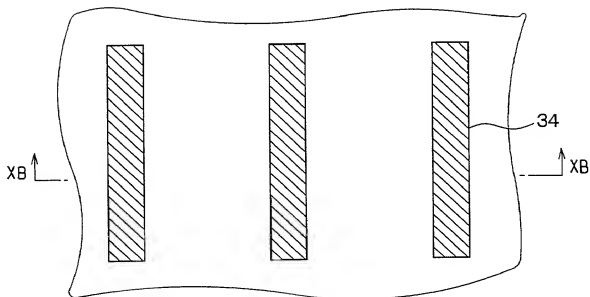
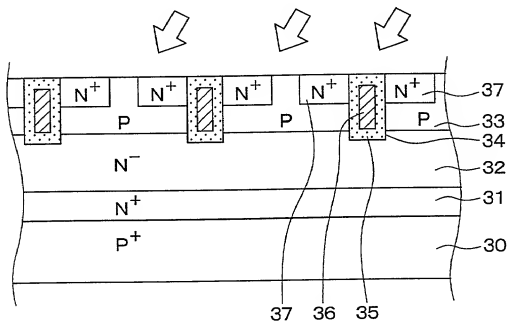


FIG. 10B



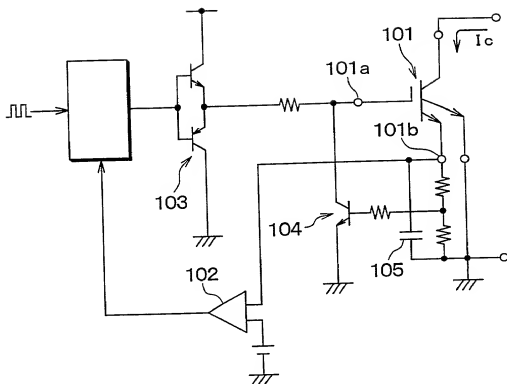
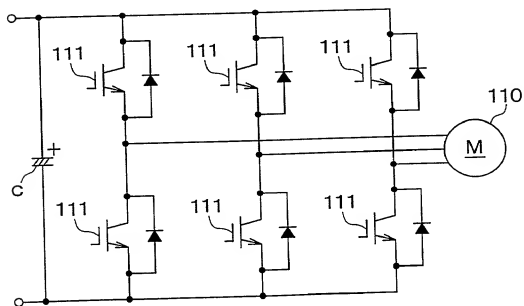
[illegible][illegible]

FIG. 13

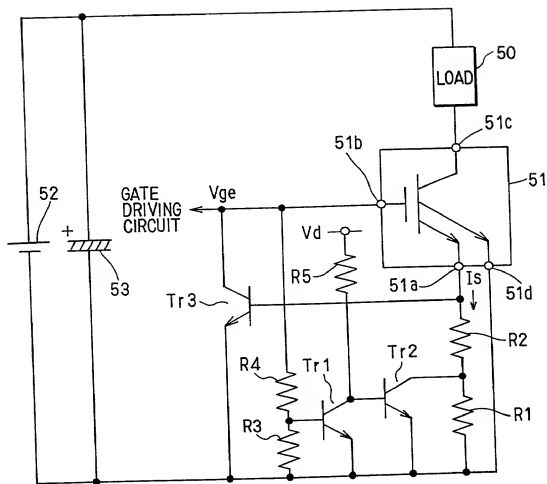


FIG. 14

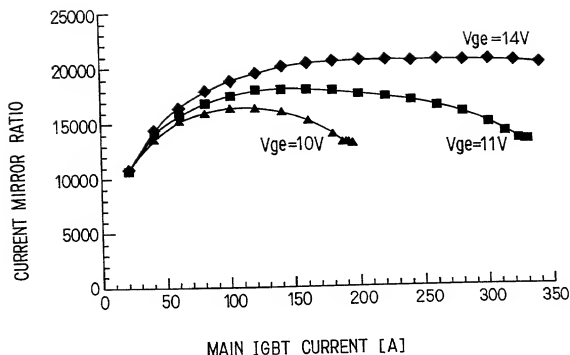


FIG. 15

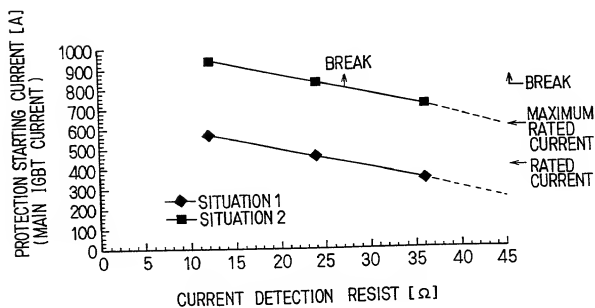


FIG. 16

